A VARIATION AWARE RESILIENT FRAMEWORK
FOR POST-SILICON DELAY VALIDATION OF
HIGH PERFORMANCE CIRCUITS

Prasanjeet Das
Prof. Sandeep Gupta (Advisor)

February 6, 2013

This research was sponsored by Intel Corporation
Can we devise a method to determine the worst case delay of the chips sampled for validation from the first-silicon batch of a design?
Delay measured on fabricated chips tend to deviate from estimated nominal delay due to

- **Multiple input switching (MIS)**
  - Increase/decrease of delay due to lower order effects.
- **Normal process variations**
  - Delay marginalities due to lack of precise fabrication control.

**The scope**

Introduction | Methods | Contributions

- Process variations
- MIS

Within scope
- hard to detect
Motivation

Increasing importance of validation

Current validation approaches inadequate

Current delay-testing approaches inadequate
**Proposed flow**

1. **Netlist** → **ATPG Framework**
2. **Delay model** → **Generate vectors**
3. **Apply vectors and measure delay**
4. **Software**
5. **Hardware**

**Methods**

- Automatic Test Equipment
- Chip

---

**Introduction | Methods | Contributions**
Bounding approximations to capture variations and MIS using bounds at low complexities.

This model captures:
- Input slew
- Input position
- Output load.
- Input skew (MIS)
- State of internal capacitances
- Process variations

Resilient model (3, 4 point bound)

Max delay of a 2-input NAND gate

MIS + Variations (126% higher delay)

Resilient delay model
Generate vectors that can account for delay increase due to MIS and process variations

Resilient model (3.4 point bound)

Region 1: Large skew (skew > $\delta$)

Region 2: Small skew (skew < $\delta$)

Region 3: Overlap

01 > 11

MIS-aware vector generator
Segment global process variation envelope to reduce test-volume and test application time

Global-only process shift can be estimated using ring-oscillator based process monitors.

Variation-aware vector generator
**Contributions**

**Systematic framework for post-silicon marginality validation**

Experiments on real-chip based benchmark:
- 5X reduction in path-set
- 2X reduction in test-generation time
- 20X reduction in test-application time
- 10% higher delay invocation

**SCAN based post-silicon marginality validation**

Silicon experiments on a processor netlist:
- Reduction in path-set
- Tests exposed unique detects
- Tests ran at lower frequency

“TEST” learns from “DESIGN”

**Short term benefits**

Variation and MIS aware delay validation framework
Introduction | Methods | Contributions

**Long term benefits**

- **Increasing importance of validation**
- **Current validation approaches inadequate**
- **Current delay-testing approaches inadequate**

**Post-silicon validation**

- 20XX onwards

**% of total design resources**


**% of ASIC Designs**

- Number of spins required: 1, 2, 3, 4 or more

**Verification**

- Perfect
- Imperfect
- Validation perfect
- Validation imperfect
- Redesign imperfect

- Motorola, Sun, NVIDIA, Intel

- Tested