A 95-MS/s 11-bit 1.36mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS

Jae-Won Nam, David Chiong, and Mike Shuo-Wei Chen

Motivation

Conventional ADC Architecture Analysis:

1. Synchronous SAR ADC
2. Asynchronous SAR ADC

3. Pipelined SAR ADC

Advantages:
- Power efficient topology
- Scanning friendly architecture
- Speed up by asynchronous clocking

Disadvantages:
- Active Amp: Power dissipation
- Passive Amp: Distortion due to non-linear parasitic cap

State-of-the-art

Applications: Future Mobile Communication Devices

Objective: Find the best power efficient ADC architecture in high-speed and high-resolution regimes.

Proposed Asynchronous SAR ADC

• Traditional Asynch. SAR ADC
  - Basic concepts for Passive Gain stage

• Proposed Asynch. SAR ADC
  - Basic operating sequences
  - Entire block diagram

Key Highlights

• Passive amplifier (Power-less)
• Comparator noise requirement
• Redundant SAR operation
• Non-linear distortion effect
• Passively amplified signal
• Comparison time

Integrated Circuit Implementation

Proposed level shifting circuit to prevent voltage over-range issue

Subsequent SAR circuits

Time-out Scheme

Chip Photograph

Measurement Results & Performance Summary

Static performances

Figure-of-Merit Chart

Dynamic performances

"Proposed Embedded Passive Gain technique enhances conventional Asynchronous SAR ADC structure's Power Efficiency in high resolution regime."