In a three-dimensional integrated circuit (3DIC), multiple active layers are stacked vertically to make a single chip. Why 3DIC? High device density, smaller chip footprint, shorter interconnects, heterogeneous integration, chip integration, etc. Tiers are interconnected using 3D-vias. A face-to-face (F2F) bonded 3DIC uses bondpoints (micro-bumps) to interconnect the tiers, while through-silicon-vias (TSVs) are used as 3D-vias that tunnel through the active layer of a tier in face-to-back (F2B) and back-to-back (B2B) bonding.

Several previously developed models estimate 3DIC average wire length using a Rents rule based approach, but they are lacking in the following ways:
- Aspect ratio of TSVs is critical for achieving acceptable yield, and due to wafer/thickness issues, the result is a TSV that is larger compared to gates
- As transistor sizes scale down, gates become smaller, but the size of TSVs may not scale down at the same rate

Hence, the estimation model must accommodate variable relative TSV sizes.

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- Presence of TSVs complicates bonding through-silicon-vias (TSVs) are used as 3D-vias that tunnel through the active layer of a tier in face-to-back (F2B) and back-to-back (B2B) bonding

TSVs are used as 3D-vias that tunnel through the active layer of a tier in face-to-back (F2B) and back-to-back (B2B) bonding. Tiers are interconnected using 3D-vias. A face-to-face (F2F) bonded 3DIC, and the number of gates \( N \), in a random logic network, which is expressed as:

\[ T = kNP \]

Where, \( k \) and \( N \), are Rent coefficient and Rent exponent, respectively.

To enable different Rents parameters for 3DIC tiers, a tier-by-tier approach that also allows for variable TSV sizes is introduced for achieving wire length estimates in 3DICs.

_Modeling the impact of TSVs on average wire length in 3DICs_

**Motivation**
- Several previously developed models estimate 3DIC average wire length using a Rents rule based approach, but they are lacking in the following ways:
  - Either consider a fixed size or ignore the space occupied by TSVs in active area
  - Aspect ratio of TSVs is critical for achieving acceptable yield, and due to wafer/thickness issues, the result is a TSV that is larger compared to gates
  - As transistor sizes scale down, gates become smaller, but the size of TSVs may not scale down at the same rate

Hence, the estimation model must accommodate variable relative TSV sizes.

**Assume that all tiers of a 3DIC have same Rent's parameters, and the number of gates \( N \), in a random logic network, which is expressed as:**

\[ T = kNP \]

Where, \( k \) and \( N \), are Rent coefficient and Rent exponent, respectively.

To enable different Rents parameters for 3DIC tiers, a tier-by-tier approach that also allows for variable TSV sizes is introduced for achieving wire length estimates in 3DICs.

**Tier-by-tier Hierarchical Approach**
- Using Rents rule for a logic circuit with \( N \) gates, the number of interconnects of length \( l \), \( I(l) \), is estimated \([Davis et. al.; TIED 1998]\).
- Using \( I(l) \), average wire length of a 3DIC is estimated as shown below, where \( I_{\text{exp}}(l) \) is the maximum possible net-length in the circuit.

\[ AW_{2D} = \frac{\text{Total Wire Length}}{\text{Total Number of Nets}} = \frac{\sum_{l=0}^{\text{Max}} I(l)}{\sum_{l=0}^{\text{Max}} I(l)} \]

- In a 3D-IC, TSVs occupy active area as shown on the right.
  - The dimensions are in gate-pitches
  - Each grid-box in the figure is a socket of one-gate size
  - A tier with \( N \) gates and \( n \) TSVs, with \( l \), \( l \), is shown
  - \( q \) is pitch of the TSVs placement, each TSV of size \( q \times q \)
  - Presence of TSVs complicates \( I(l) \) estimation
  - Maximum possible length is \((2L-1)\).

- In \( l \)-th tier of a 3DIC, the distribution of interconnects between gates only, \( I(l) \), is estimated, then 3DIC average wire length is given by

\[ \text{Total number of connections between gates only} \]

\[ AW_{2D} = \frac{\sum_{l=0}^{\text{Max}} I(l)}{\sum_{l=0}^{\text{Max}} I(l)} + \frac{\sum_{l=0}^{\text{Max}} I(l)}{\sum_{l=0}^{\text{Max}} I(l)} + \frac{\sum_{l=0}^{\text{Max}} I(l)}{\sum_{l=0}^{\text{Max}} I(l)} \]

**Results**

- **3 experiments were conducted to demonstrate the utility of the model**
  - A 2-tier 3DIC configuration is used for easier understanding
  - However, the model is applicable to a 3DIC with any number of tiers

1. A circuit with 10M gates; \( p=0.75 \), and \( f=1 \) was used
2. Tested for three different TSV sizes \((tsv)\), and for both F2B and B2B bonding
3. Upper bound \((NTSV)\) is found and the results are presented in the table below

**Conclusions**

- **A tier-level hierarchical approach based on Rents rule is introduced for estimating 3DIC average wire length**
- Discrete wire length distribution of each tier is estimated independently to provide the ability to handle tiers with different Rents parameters
- Applicable for variable TSV dimensions and for all bonding techniques
- **Future work:** Model will be further validated against 3DIC designs and will be used to estimate other performance metrics