Introduction & Motivation

- FPGA
  - Configurable logic block
  - Programmable interconnect
- Parameterized Architecture
  - Algorithm-mapping parameters
  - Architecture-binding parameters
- Multiple Objectives
  - Energy-efficient designs
  - High throughput designs
- Exponentially Large Design Space
- Current Work
  - 12 to 14 days for 1 million design points
  - Target:
    - 1 million design points in a few hours
    - >5000 design points per minute

Design Space Exploration

- High level performance model based design space exploration
- Model refinement to incorporate interconnect power and improve accuracy
- Design framework to perform design space exploration and Pareto set generation
- Evaluation: Comparison of generated promising designs with simulated results

Results and Future Work

- Applications
  - Image Convolution
  - Convolutional Neural Network
- Image Convolution: 77% overlap of estimated designs and simulated designs
- Convolutional Neural Network: Similar trends in simulated and estimated Pareto optimal designs
- Future work
  - Develop heuristics for interconnect power estimation
  - Use learning and classification techniques for interconnect modeling.